REMARKS

Claims 1-23 are pending in this application, of which claims 2-20 have been withdrawn from consideration and claims 1 and 21 have been amended. No new claims have been added.

Claims 1 and 21-23 stand rejected under 35 USC §102(e) as anticipated by U.S. Patent 6,379,782 to Iguchi et al. (hereinafter "**Iguchi et al. '782**").

Applicant respectfully traverses this rejection.

Iguchi et al. '782 discloses a semiconductor device formed with metal wiring on a wafer. An insulating layer is formed on a whole surface of a wafer. Recesses such as wiring grooves are formed in the insulating layer. A part of the insulating layer is removed on a region whose distance from the peripheral edge of the wafer is a value x or less. After a conductive film is formed on the whole wafer surface, a part is removed on a region whose distance from the peripheral wafer edge is a value y ($y<x$) or less.

The Examiner urges **Iguchi et al. '782** has a peripheral multi-layer structure comprising a conductor pattern filling each of the trenches and made of a same material as said wiring patterns in associated one of said interlevel insulating films and not having conductor patterns corresponding to said via conductors. Applicant respectfully disagrees, and respectfully submits that there can be found no plausible ground to determine that **Iguchi et al. '782** has no via conductors in the peripheral multi-layer structure.

Iguchi et al. '782 shows multi-layer wiring in Fig. 6 and discusses the problem of film peeling, and discloses that copper in the peripheral region should be removed (column 10). The

multi-layer wiring structure includes conductive plugs 43 and Cu wiring patterns 44. However, the description of the embodiments does not refer to the formation of any conductive plugs. The first embodiment describes "copper wiring forming process based on a damascene process". The terms "wiring grooves" and "wiring pitch" should be interpreted that the wirings shown in Figs. 7 to 21 are not limited to the peripheral portion. The first and second embodiments describe how the copper wiring patterns are made, but no description is made how the conductive plugs are made (e.g., see Figs. 7A to 7F). Applicant's basic concept of forming damascene wiring containing wiring patterns in the trenches and via conductor in the via hole in the circuit area, and damascene wiring structure containing only wiring patterns in the trenches but no via conductors in the peripheral region is neither disclosed nor suggested in **Iguchi et al. '782**.

Claim 21 has been amended to recite "a first insulating layer having a lower dielectric constant than silicon oxide, [[and]] formed over said underlying structure in an area excepting a peripheral area of said underlying structure, and having gradual decreasing thickness at its periphery". Figs. 6A-6D clearly show such a configuration of the SiLK layer 112. In contrast, the HSQ of **Iguchi et al. '782** has a sharp edge, as shown in Fig. 15D, and is disclosed to be formed by etching (column 13, lines 19-29).

Thus, the 35 USC §102(e) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, claims 1 and 21-23, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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